each the pixel electrode. a voltage on the pixel electrode can be constant. Therefore, image quality can be improved.

What is claimed is:

Sub B2

1. A liquid crystal display device comprising:

first and second substrates each having an insulating surface;

at least one pixel electrode arranged on the first substrate at a matrix form;

an opposite electrode arranged on the second substrate;

a liquid crystal disposed between the first and second substrates; and

at least one digital memory circuit which is constructed by thin film transistors, wherein the digital memory circuit is connected with the pixel electrode and stores a binary information;

wherein a voltage is directly applied to said pixel electrode through said digital memory circuit based on said binary information,

wherein said liquid crystal display device includes a time gradation display device.

2. The device of claim 1 wherein a voltage having an amplitude equivalent to that of the voltage stored in the digital memory circuit is supplied to the opposite electrode.

3. The device of claim 1 wherein the number of pixel electrodes equals to the number of the digital memory circuit.

4. The device of claim 1 wherein the liquid crystal display device includes a digital gradation display device.

5. The device of claim 1 wherein the voltage includes one of a high voltage and a low voltage.

Sub A2

6. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrate, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said thin film transistor, wherein said memory circuit stores an information output by said thin film transistor; and

at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode,

wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit.

7. The active matrix display device of claim 6 further comprising an opposite electrode on the other of said substrates,

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Sub A3

8. The active matrix display device of claim 6 wherein the number of pixel electrodes equals to the number of the memory circuit.

9. The active matrix display device of claim 6 wherein the active matrix display device includes a digital gradation display device.

10. The active matrix display device of claim 6 wherein the active matrix display device includes a time gradation display device.

11. The active matrix display device of claim 6 wherein the different voltages include a high voltage and a low voltage.

Sub a4

12. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrate, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and

at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode,

wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least second and third thin film transistors,

one of source or drain of the second thin film transistor being connected with one of said signal lines, a gate electrode of the third thin film transistor, and one of source or drain of the first thin film transistor,

the other of source or drain of the second transistor being connected with the other of said signal lines and one of source or drain of the third thin film transistor, and

a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, one of said signal lines, and said electro-optical modulating layer.

13. The active matrix display device of claim 12 wherein a voltage supplied to the the electro-optical modulating layer is substantially zero on time average.

14. The active matrix display device of claim 12 wherein the number of pixel electrodes equals to the number of the memory circuit.

15. The active matrix display device of claim 12 wherein the active matrix display device includes a digital gradation display device.

16. The active matrix display device of claim 12 wherein the active matrix display device includes a time gradation display device.

17. The active matrix display device of claim 12 wherein the different voltages include a high voltage and a low voltage.

Sub a5

18. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrate, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor,

wherein said memory circuit stores an information output by said first thin film transistor; and

at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode,

wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least two invertors, said invertors comprising at least two thin film transistors and being connected with said signal lines.

19. The active matrix display device of claim **18** wherein the number of pixel electrodes equals to the number of the memory circuit.

20. The active matrix display device of claim **18** wherein the active matrix display device includes a digital gradation display device.

21. The active matrix display device of claim **18** wherein the active matrix display device includes a time gradation display device.

22. The active matrix display device of claim **18** wherein the different voltages include a high voltage and a low voltage.

23. The active matrix display device of claim **18** further comprising an opposite electrode on the other of said substrates,

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Sub a6

24. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrate, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and

at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode,

wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least two thin film transistors, having a same conductivity type.

25. The active matrix display device of claim 24 wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average.

26. The active matrix display device of claim 24 wherein the number of pixel electrodes equals to the number of the memory circuit.

27. The active matrix display device of claim 24 wherein the active matrix display device includes a digital gradation display device.

28. The active matrix display device of claim 24 wherein the active matrix display device includes a time gradation display device.

29. The active matrix display device of claim 24 wherein the different voltages include a high voltage and a low voltage.

30. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel; and

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

31. The method according to claim 30 wherein an output terminal of said memory circuit is connected to said pixel electrode.

32. A method of operating an active matrix display device comprising the steps of:

supplying a data through a switching thin film transistor provided at one pixel to a memory circuit;

storing said data in a memory circuit provided at said pixel;

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

33. The method according to claim 32 wherein an output terminal of said memory circuit is connected to said pixel electrode.

34. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel; and

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate, and wherein a power source voltage of said memory circuit is an alternating voltage.

35. The method according to claim 34 wherein an output terminal of said memory circuit is connected to said pixel electrode.

36. A method of operating an active matrix display device comprising the steps of:

supplying a data through a switching thin film transistor provided at one pixel to a memory circuit;

storing said data in a memory circuit provided at said pixel;

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate, and wherein a power source voltage of said memory circuit is an alternating voltage.

37. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel; and

supplying one of high and low voltages to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

38. The method according to claim 37 wherein an output terminal of said memory circuit is connected to said pixel electrode.

39. An active matrix display device comprising:

a substrate having an insulating surface;

at least one signal line and at least one scanning line extending across said signal line over said substrate wherein a pixel is defined by said signal line and said scanning line;

a switching element disposed at an intersection of said signal line and said scanning line;

a memory circuit electronically connected to said switching element; and

a pixel electrode disposed in said pixel,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

40. An active matrix display device according to claim 39 wherein an output terminal of said memory circuit is connected to said pixel electrode.

41. An active matrix display device according to claim 39 wherein said display device is a liquid crystal device.

42. The method according to claim 30 wherein said display device is a liquid crystal device.

43. The method according to claim 32 wherein said display device is a liquid crystal device.

44. The method according to claim 34 wherein said display device is a liquid crystal device.

45. The method according to claim 36 wherein said display device is a liquid crystal device.

46. The method according to claim 37 wherein said display device is a liquid crystal device.